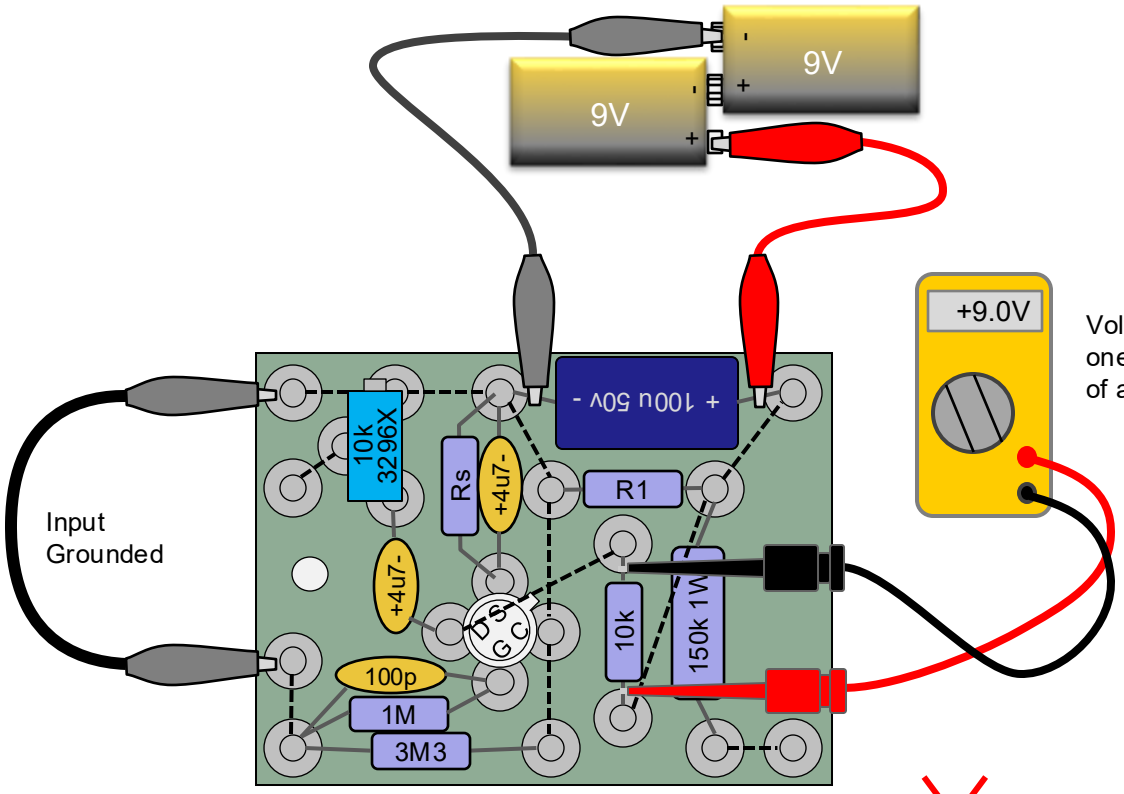
ODS FET Setup Using 9V Batteries



Voltage across Rd is one-half to one-third of applied voltage

B+5 not connected to FET board when on battery power

- Choose voltage divider resistor R1:
  - 18k for high Vd (clean boost)
  - 8k2 for low Vd (reduced headroom, increased FET Distortion)
- Connect a 10k pot in place of source resistor Rs
- For high Vd, apply +18V Vdd using series-connected 9V batteries across R1
- For low Vd, apply +9V Vdd using a single 9V battery across R1
- Adjust Rs pot for Vdd/Vd = 2.0 for high Vd, 3.0 for low Vd (Rs will typically be ~2-4k)
- Measure pot value and replace with a fixed resistor for Rs
- Connect FET board to chassis ground and B+5 (~300V)
- Verify Vdd and Vdd/Vd are in the desired ranges

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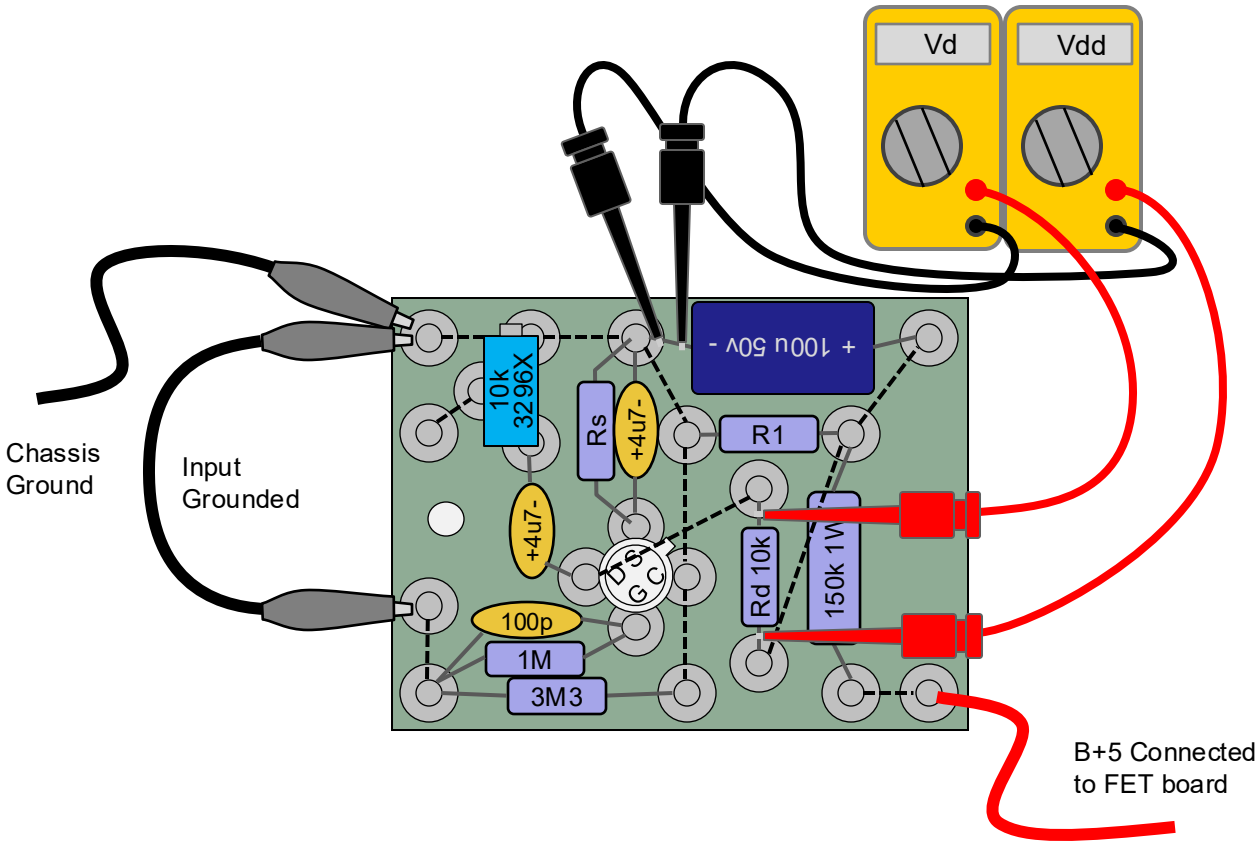
ODS FET Setup Using B+5



- Choose value for voltage divider resistor R1:
  - 18k for high Vd (clean boost)
  - 8k2 for low Vd (reduced headroom, increased FET distortion)
- Connect a 10k pot in place of source resistor Rs
- Connect chassis ground and B+5 (~300V) to FET board
- Adjust 10k Rs pot for Vdd/Vd = 2.0 for maximum headroom, or up to 3.0 for more FET distortion content (Rs range will typically be ~2-4k)
- Measure Rs pot value and replace with fixed resistor for Rs

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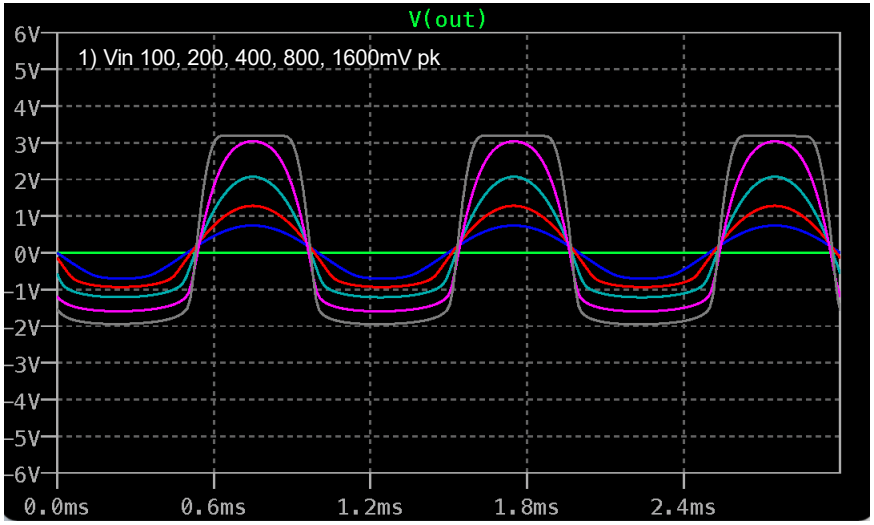
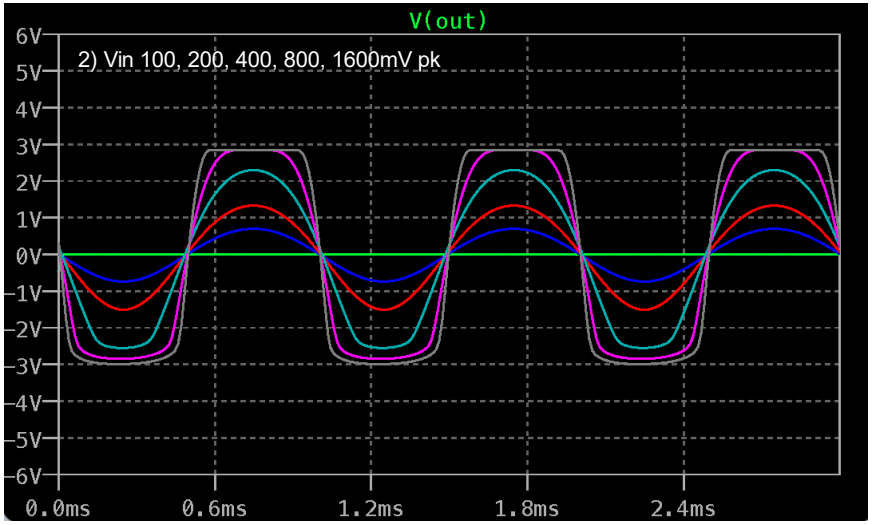
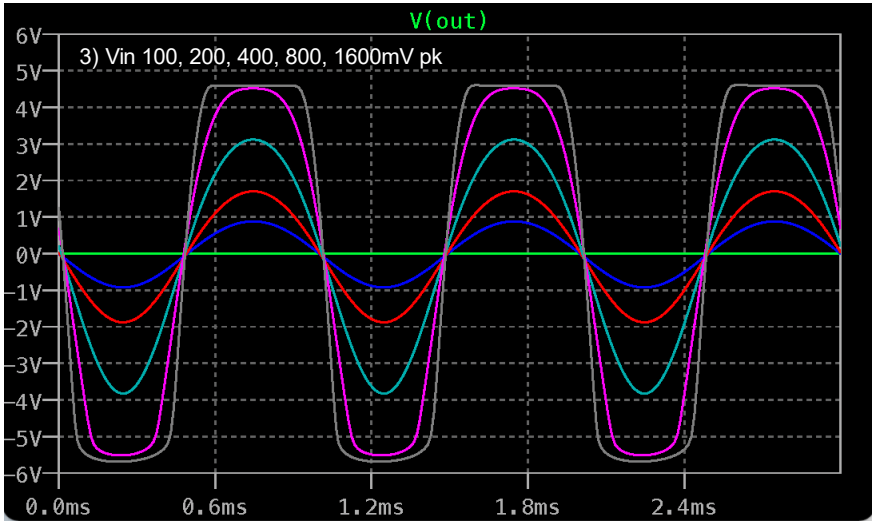
Bias and Vdd Effect on ODS FET Output Waveform at Constant B+5 Voltage

Case 1: Based on voltage measurements from a Dumble amp with NTE452 FET (2N4416 simulation is a close match).
Case 2: Same configuration as Case 1 with Rs adjusted to drop half of supply voltage across Rd (Vdd/Vd = 2) to center bias.
Case 3: B+5 divider adjusted to get ~18V Vdd, Rs adjusted to get Vdd/Vd = 2 for center bias.







FET	2N4416		
Case	1	2	3
B+5	304	304	304
R	150k	150k	150k
R1	8k2	8k2	18k
Rd	10k	10k	10k
Rs	3k3	4k07	2k32
Vd	3.72	5.67	8.79
Vdd	10.49	11.35	17.91
Vdd/Vd	2.82	2.00	2.04
Vs	2.24	2.3	2.12
1kHz Gain, dB	18	17.4	19.2
THD, % (Vin 200mV)	16.56	5.89	4.44
-3dB, Hz	63	57	72
		MPManning	2021.01.30